REPLACEMENT SHEET
Application No.: 10/606,419
Title: System and Method for Guiding and
Optimizing Formal Verification for a Circuit
Design
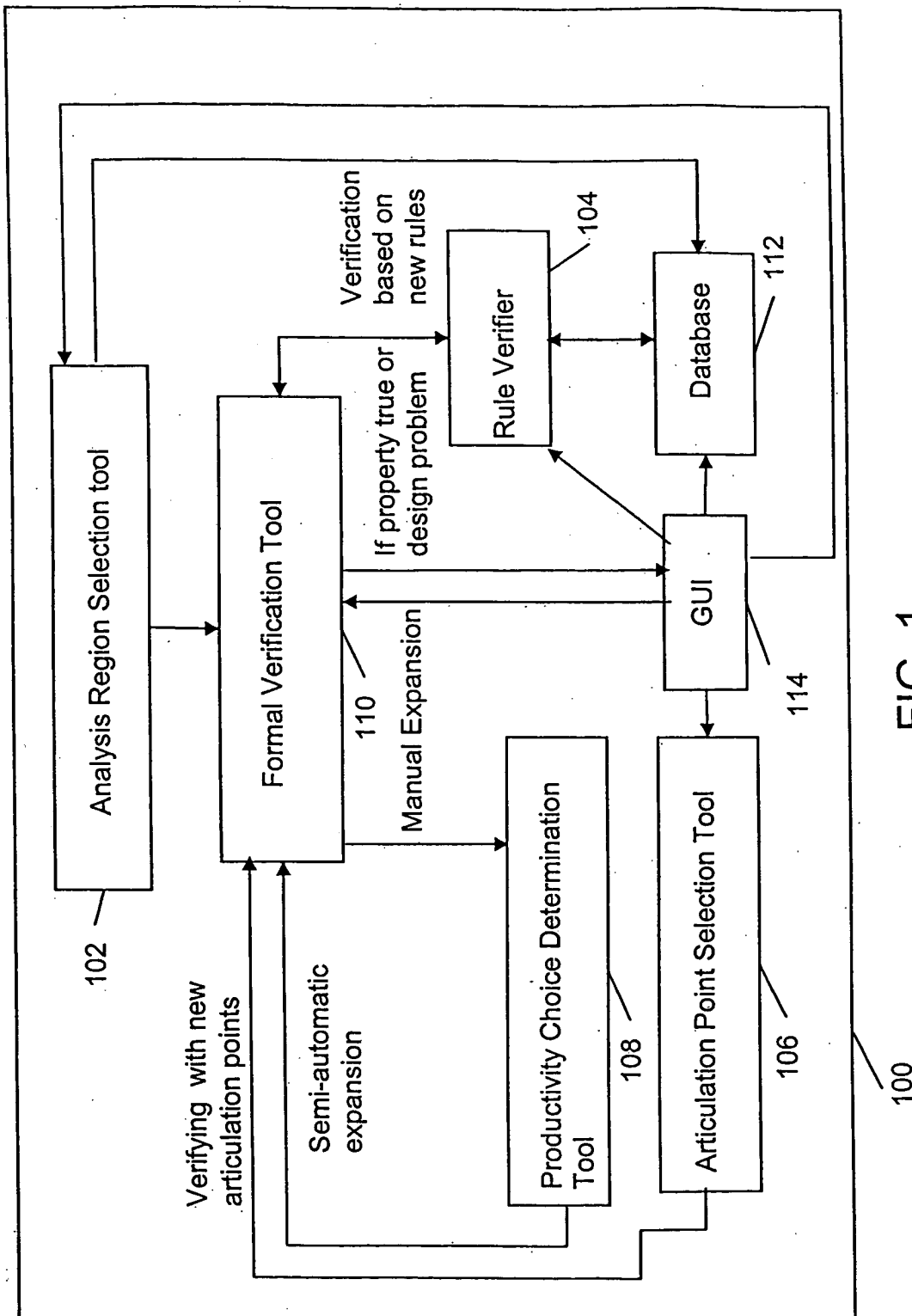Inventor(s): Vigyan Singhal et al.
Atty. Docket No.: 24006-08742

FIG. 1

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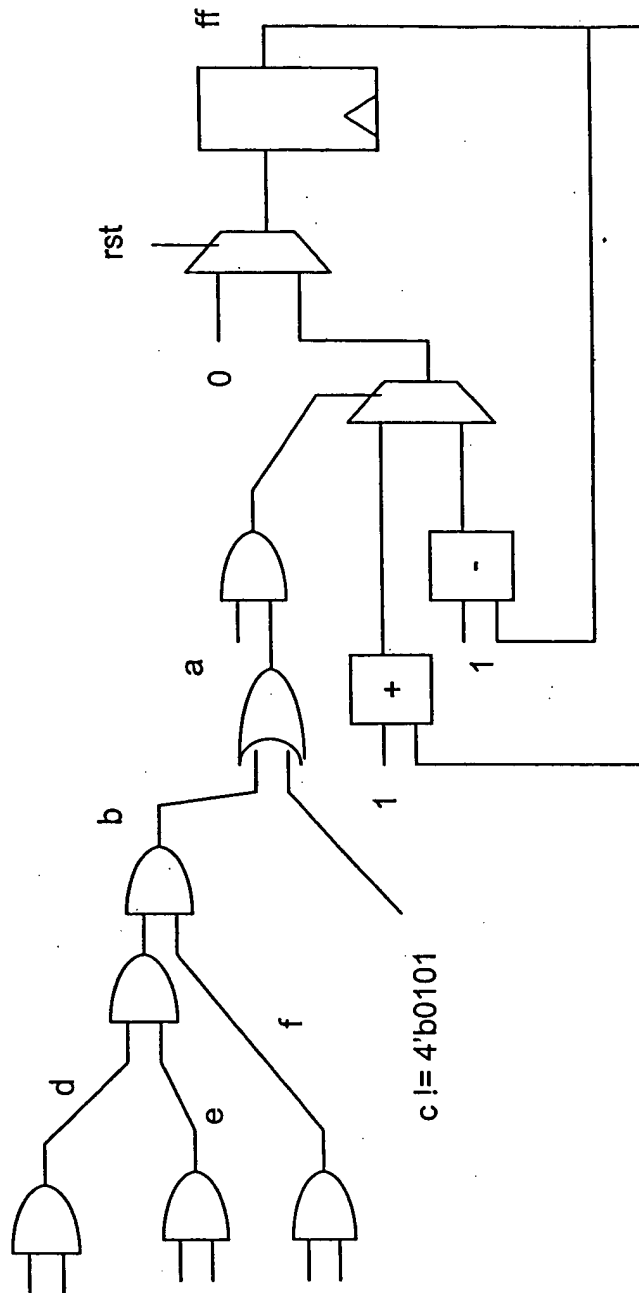Atty. Docket No.: 24006-08742

FIG. 2

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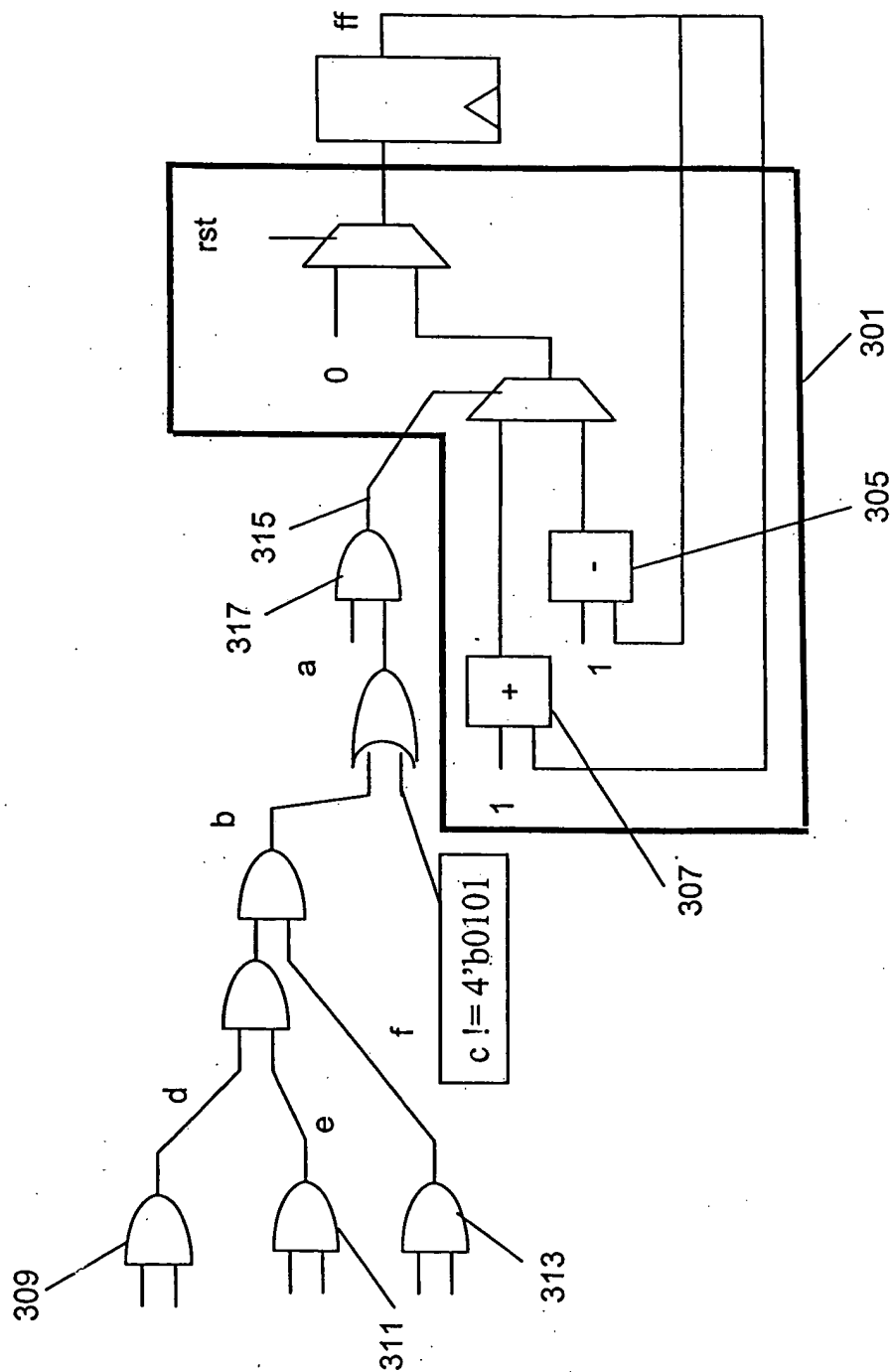Atty. Docket No.: 24006-08742

FIG. 3

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Design
Inventor(s): Vigyan Singhal et al.
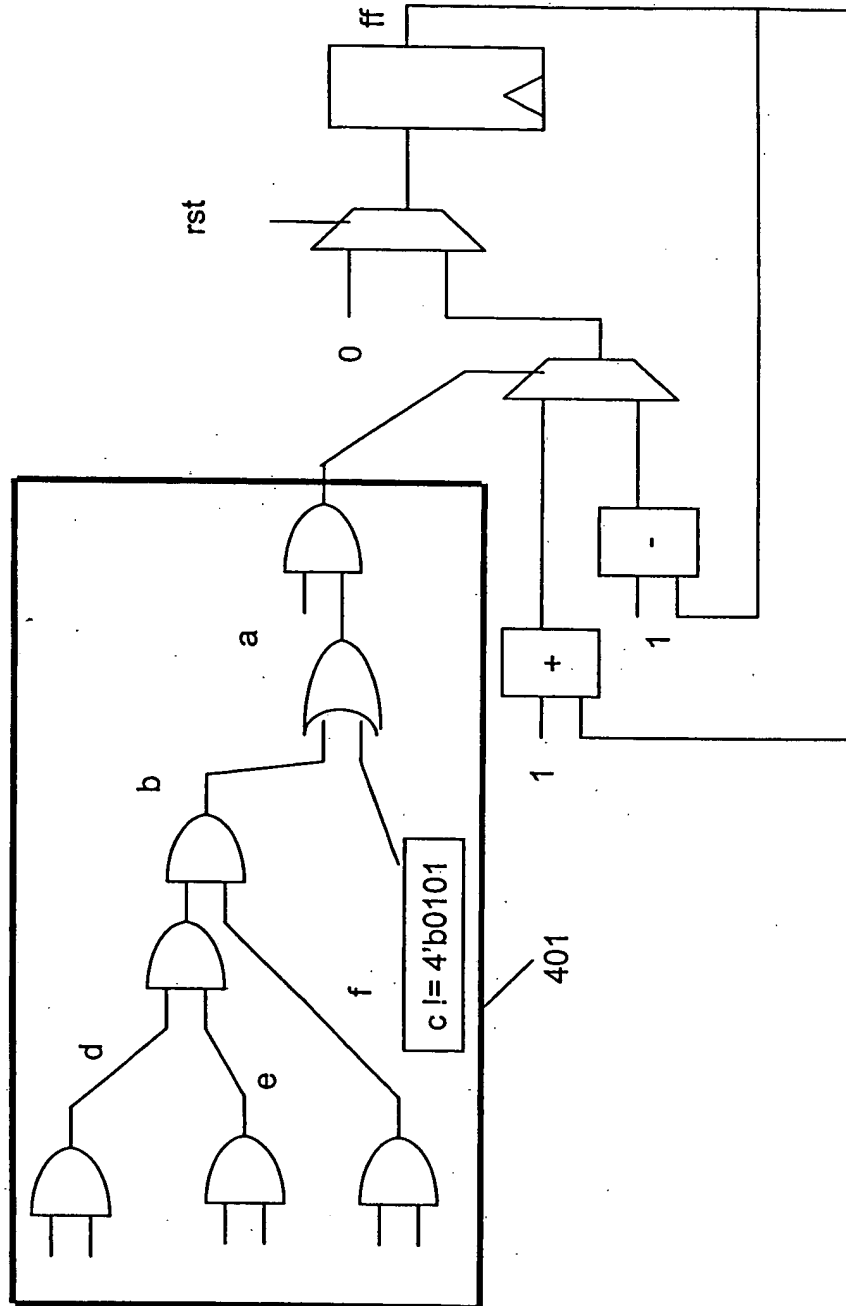Atty. Docket No.: 24006-08742

FIG. 4

REPLACEMENT SHEET
Application No.: 10/606,419
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Design
Inventor(s): Vigyan Singhal et al.
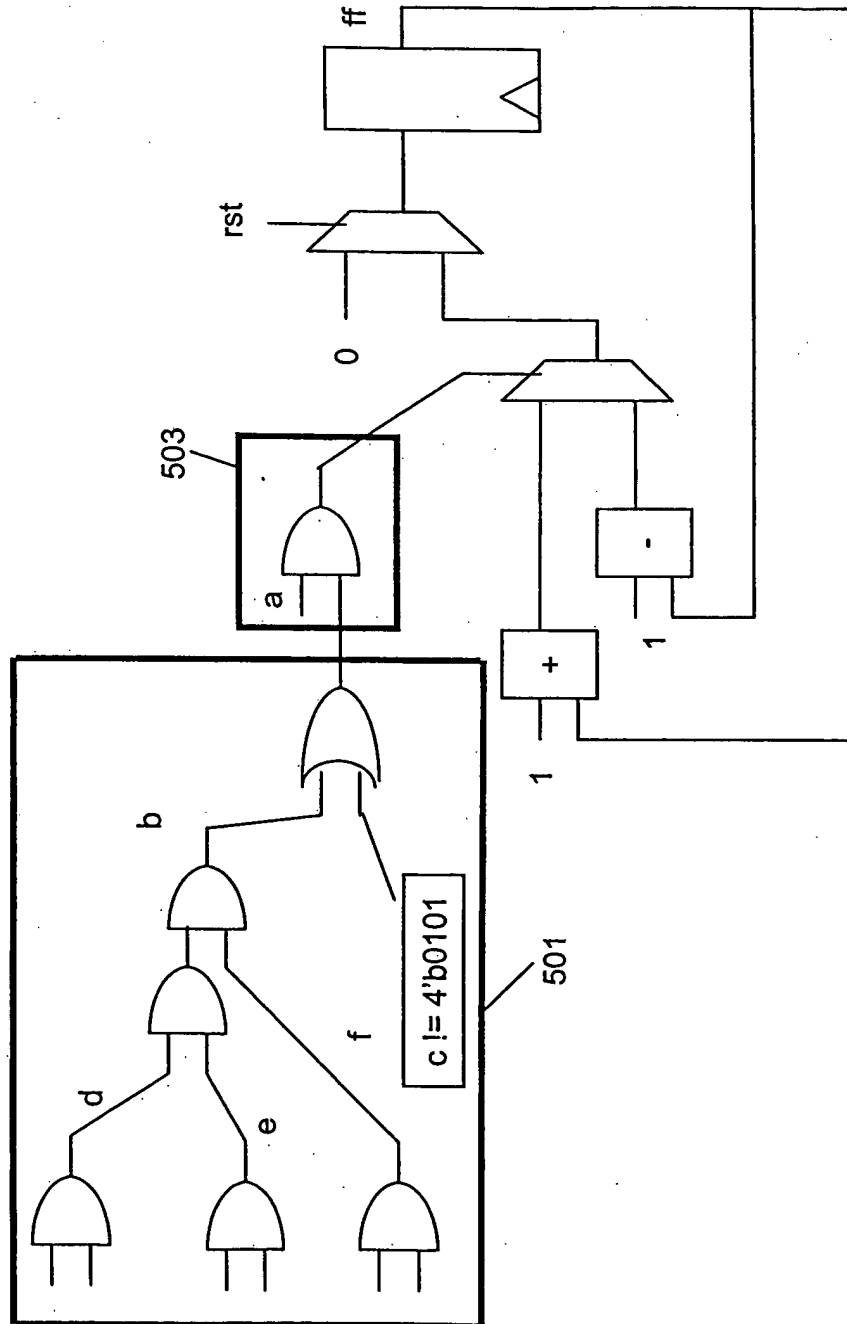Atty. Docket No.: 24006-08742

FIG. 5

REPLACEMENT SHEET
Application No.: 10/606,419
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Design
Inventor(s): Vigyan Singhal et al.
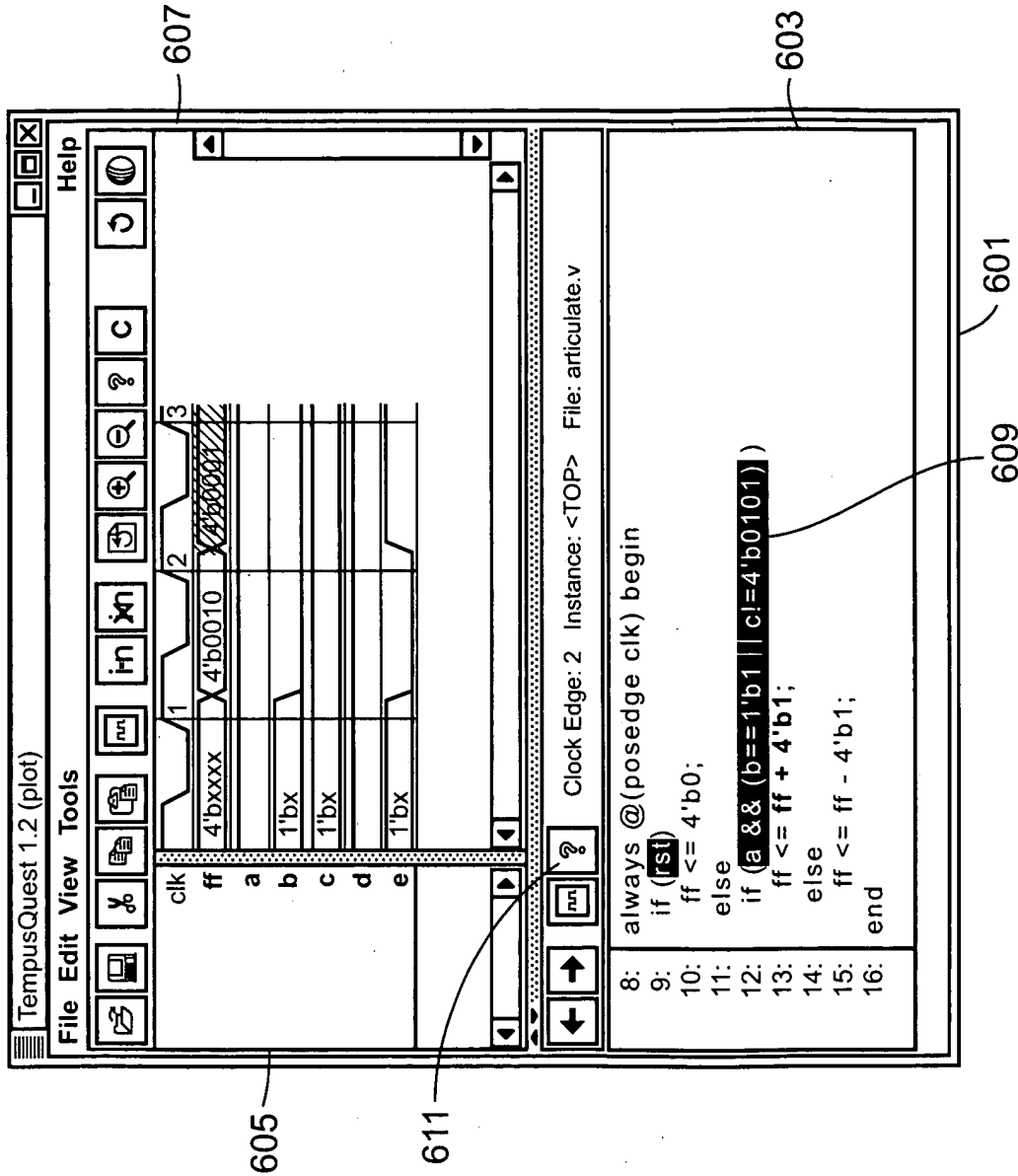Atty. Docket No.: 24006-08742

FIG. 6

REPLACEMENT SHEET
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Design
Inventor(s): Vigyan Singhal et al.
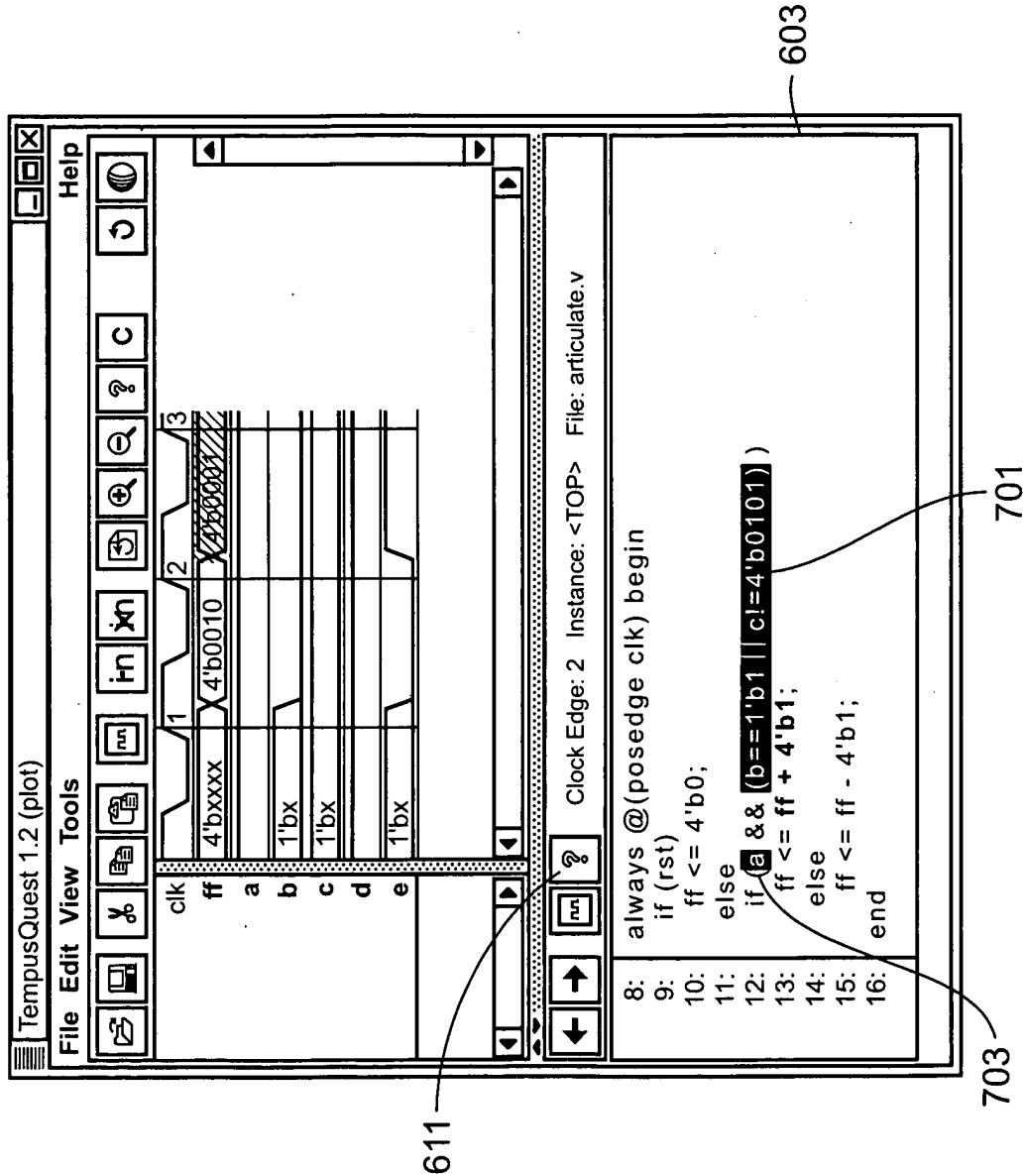Atty. Docket No.: 24006-08742

FIG. 7

REPLACEMENT SHEET
Application No.: 10/606,419
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Optimizing Formal Verification for a Circuit
Design
Inventor(s): Vigyan Singhal et al.
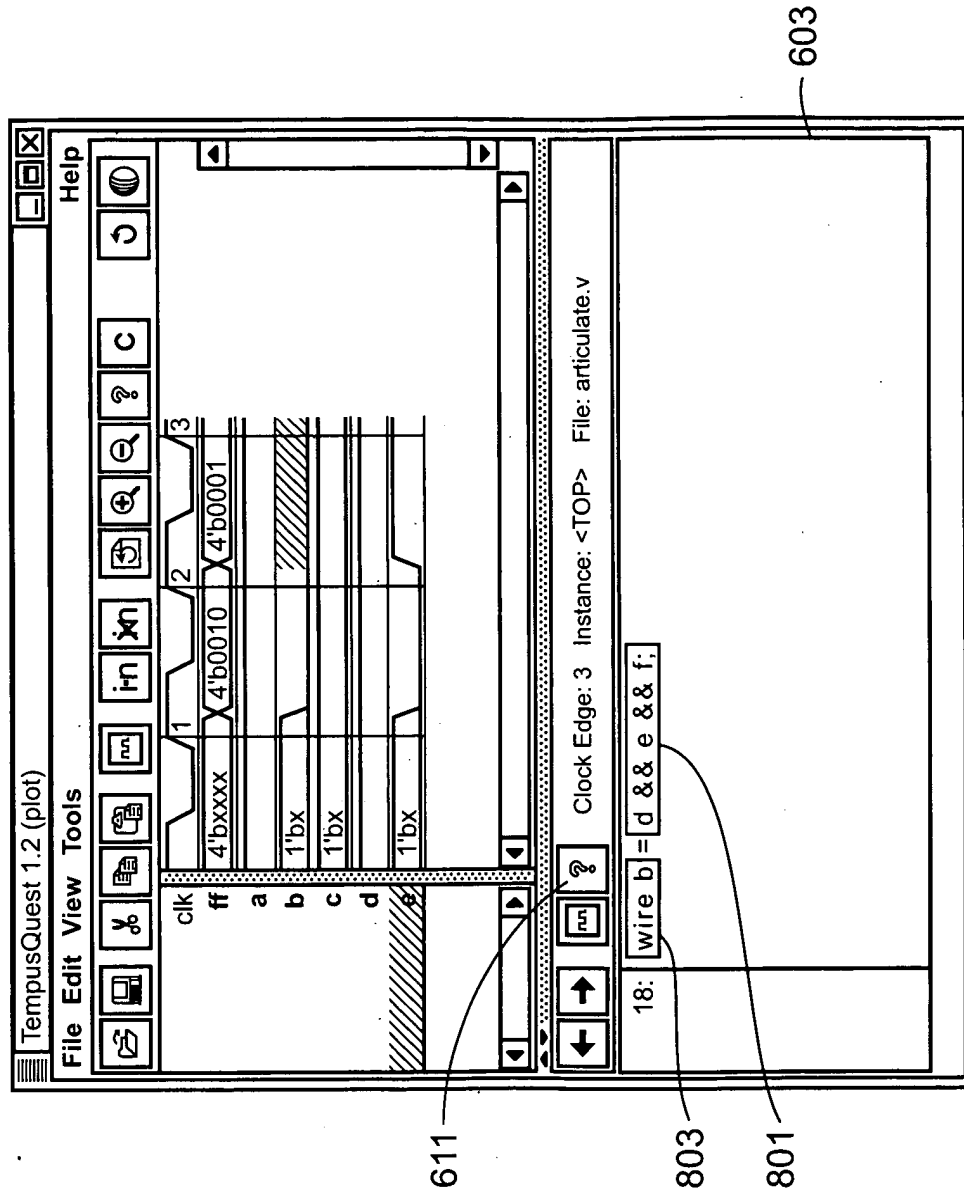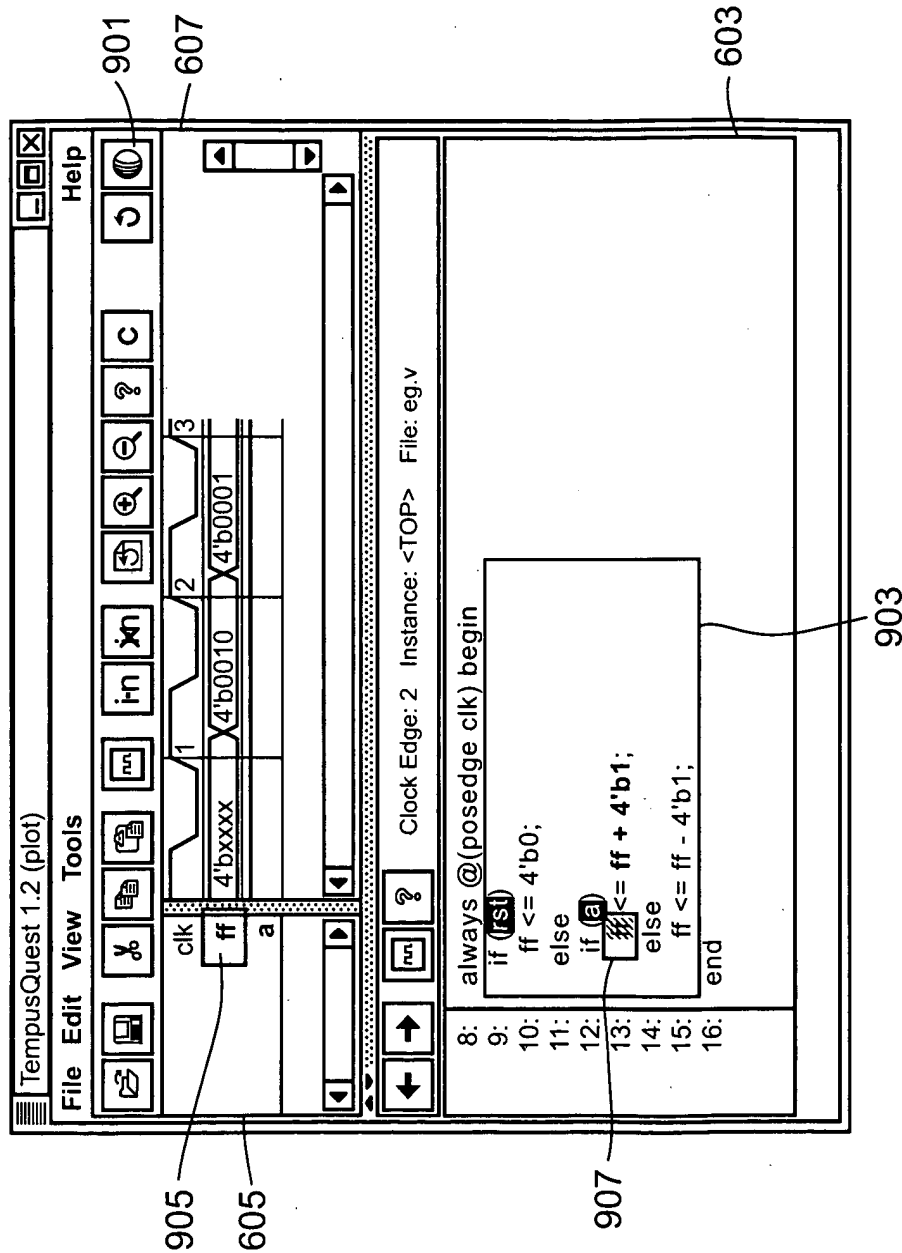Atty. Docket No.: 24006-08742

FIG. 8

REPLACEMENT SHEET
Application No.: 10/606,419
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Optimizing Formal Verification for a Circuit
Design
Inventor(s): Vigyan Singhal et al.
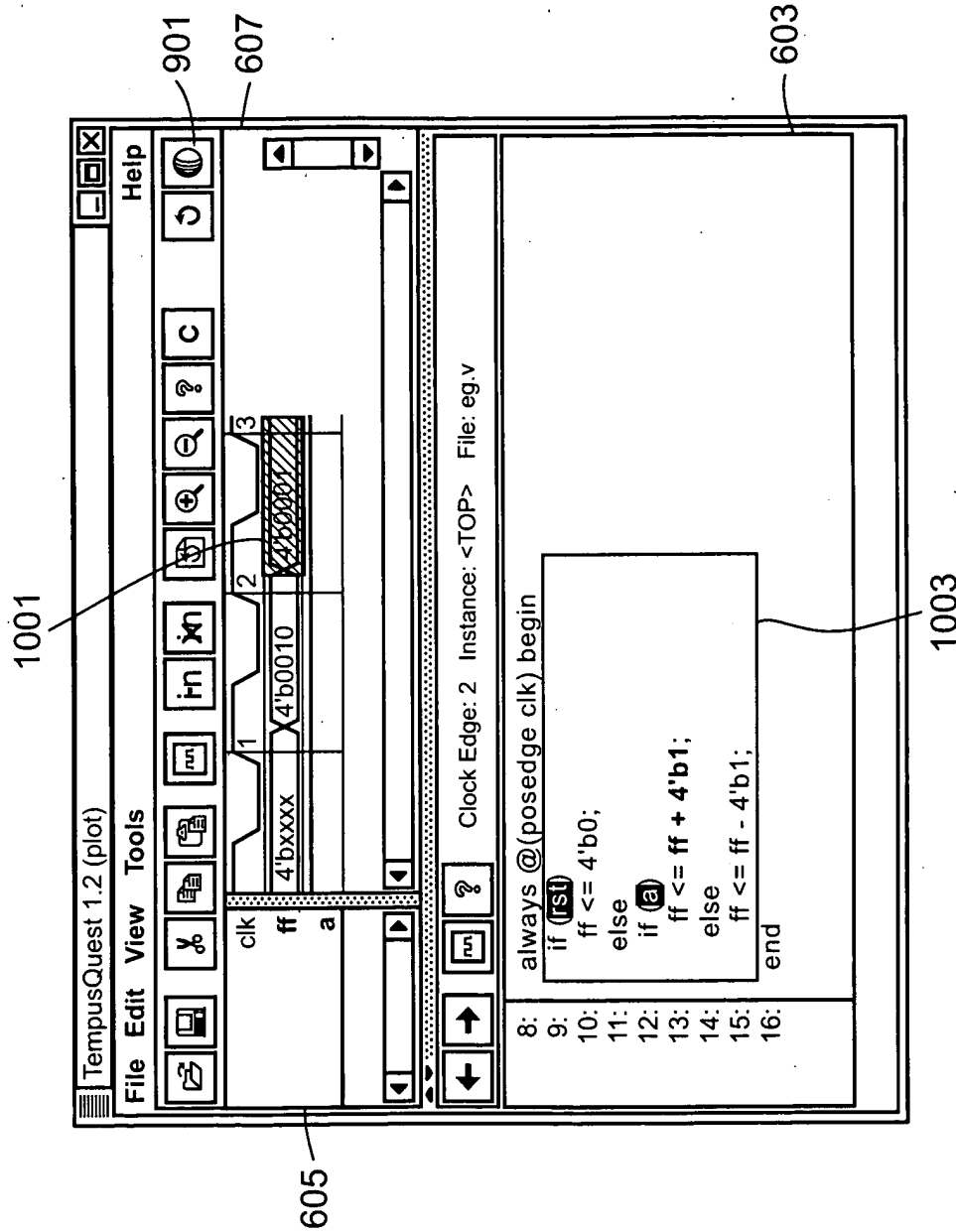Atty. Docket No.: 24006-08742

FIG. 9

REPLACEMENT SHEET
Application No.: 10/606,419
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Optimizing Formal Verification for a Circuit
Design
Inventor(s): Vigyan Singhal et al.
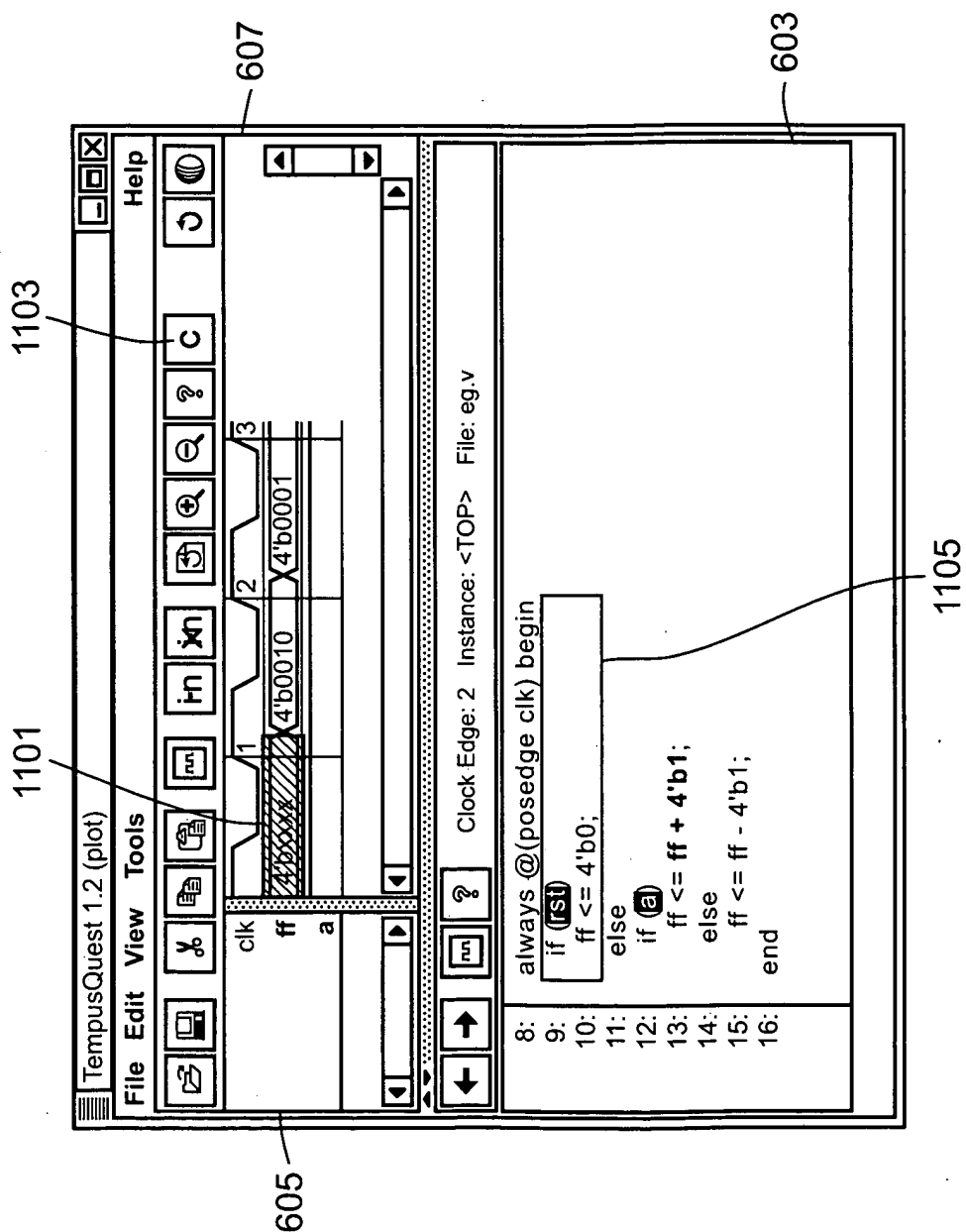Atty. Docket No.: 24006-08742

FIG. 10

REPLACEMENT SHEET
Application No.: 10/606,419
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Design
Inventor(s): Vigyan Singhal et al.
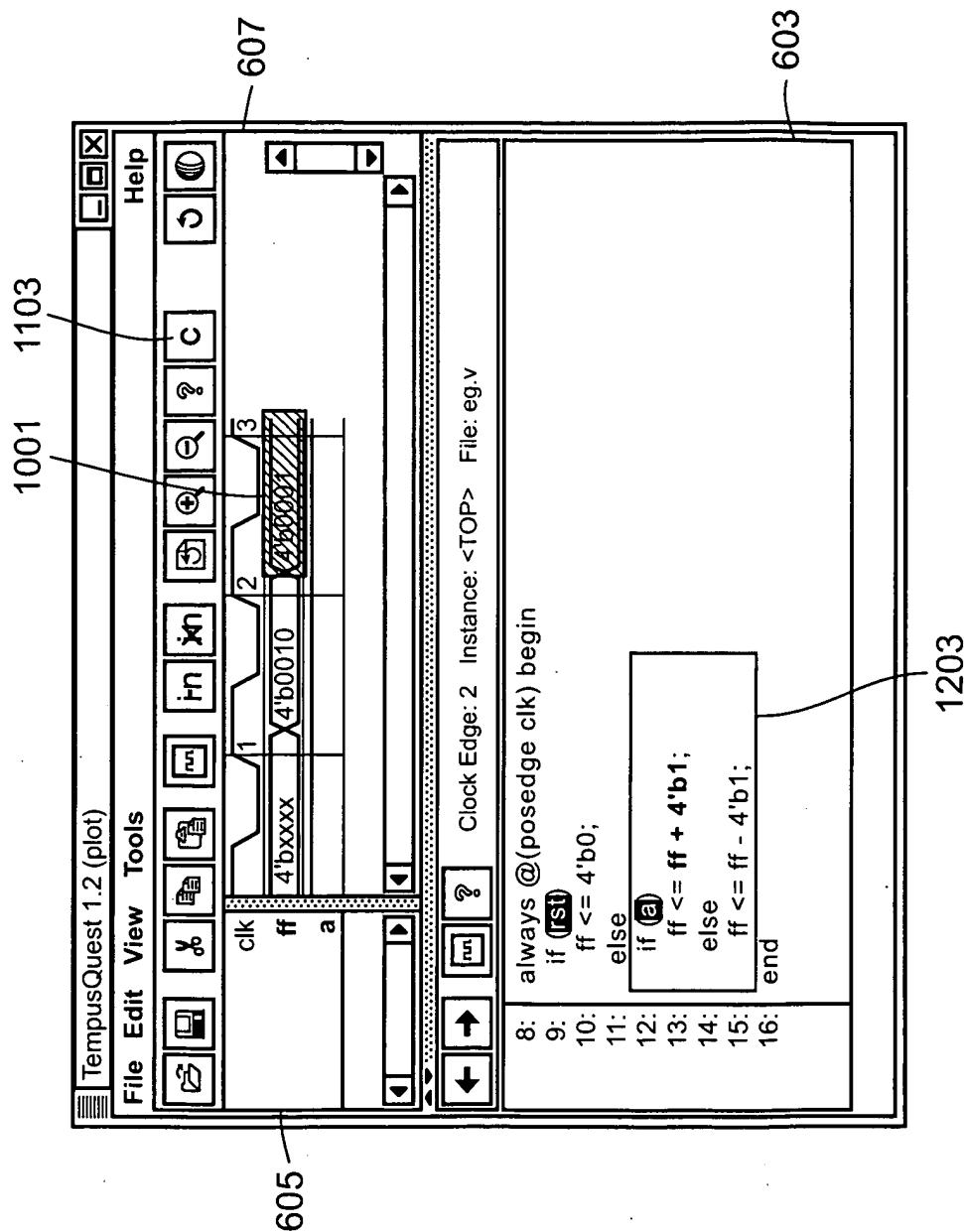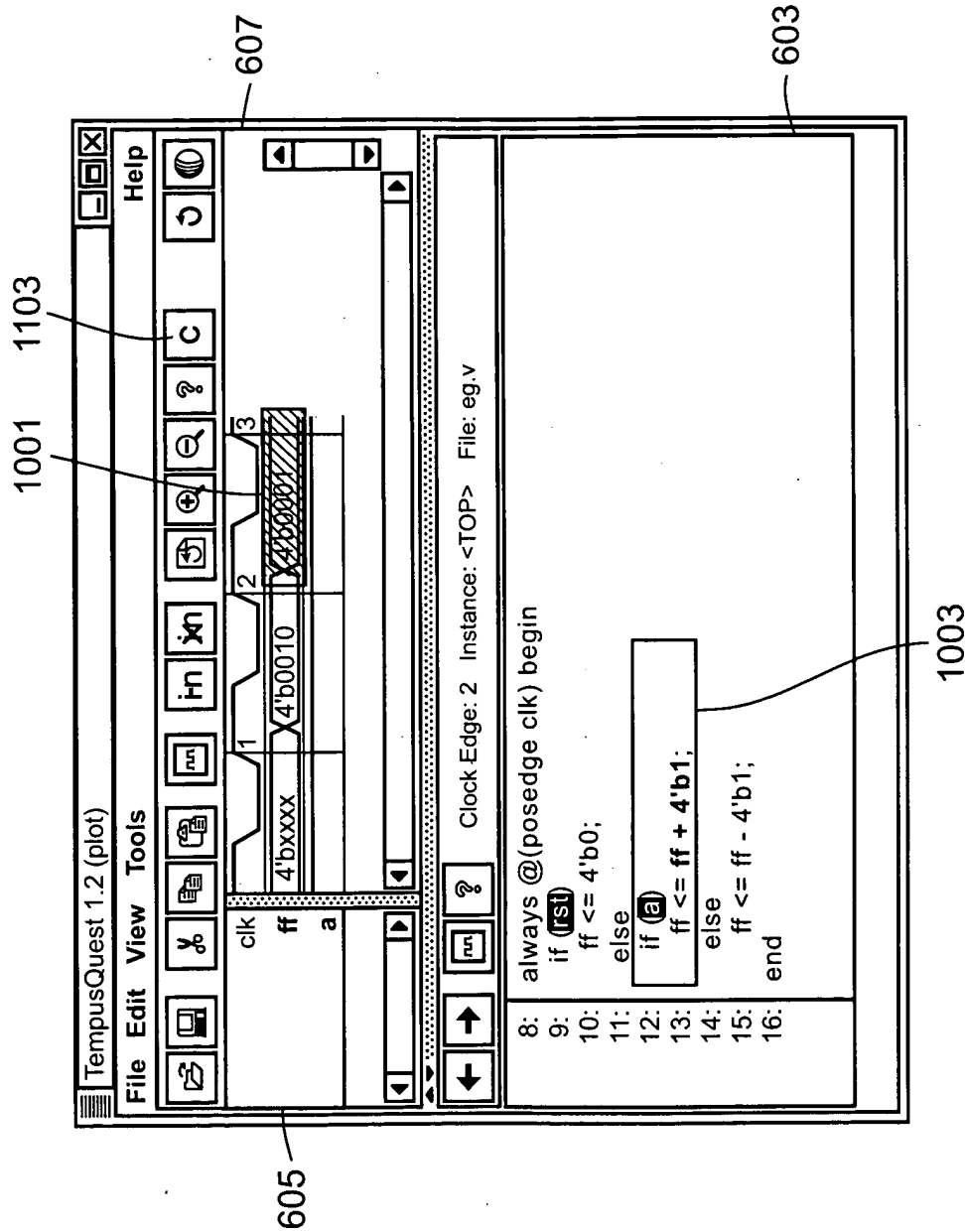Atty. Docket No.: 24006-08742

FIG. 11

FIG. 12

REPLACEMENT SHEET
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Optimizing Formal Verification for a Circuit
Design
Inventor(s): Vigyan Singhal et al.
Atty. Docket No.: 24006-08742

FIG. 13

FIG. 14

REPLACEMENT SHEET
Application No.: 10/606,419
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Design
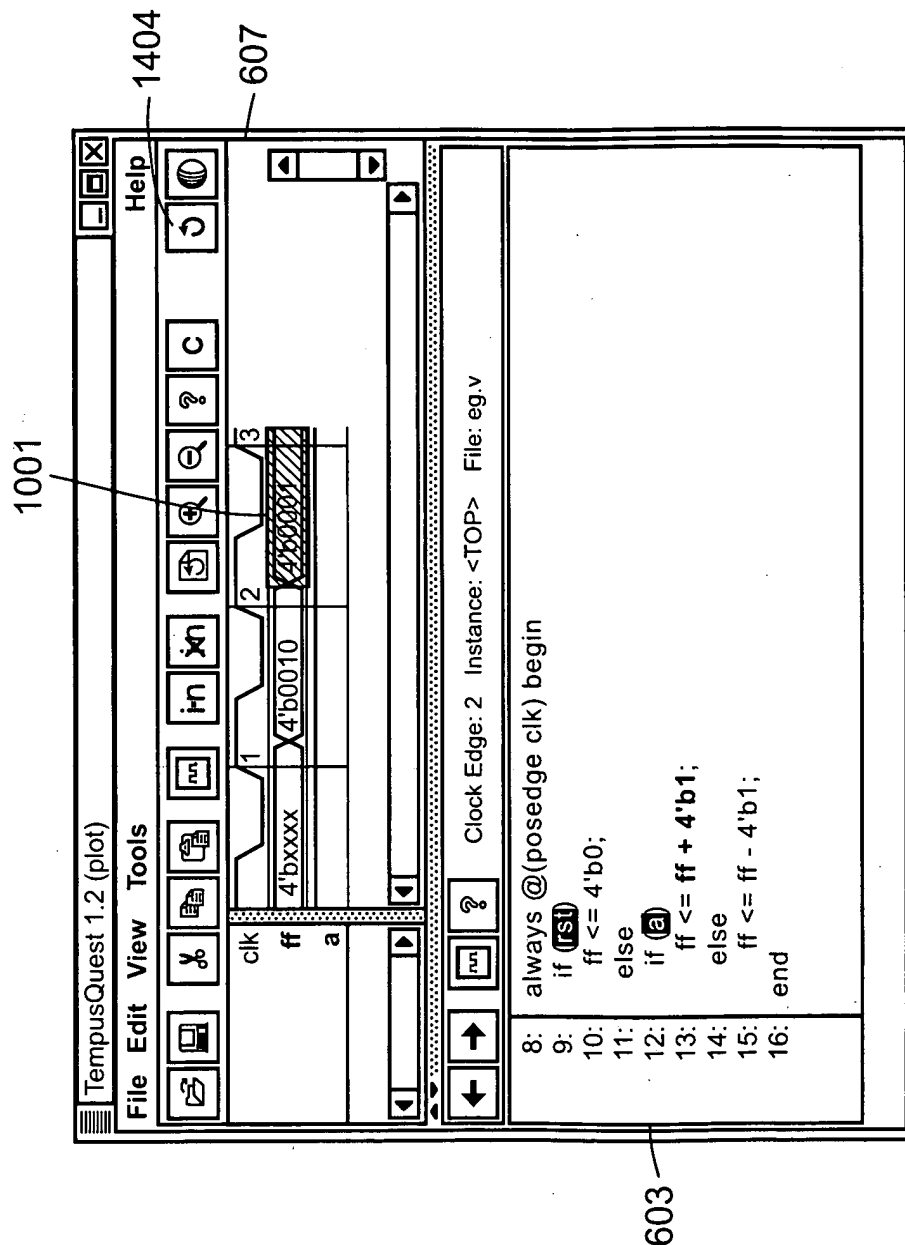Inventor(s): Vigyan Singhal et al.
Atty. Docket No.: 24006-08742

FIG. 15

REPLACEMENT SHEET
Application No.: 10/606,419
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Design
Inventor(s): Vigyan Singhal et al.
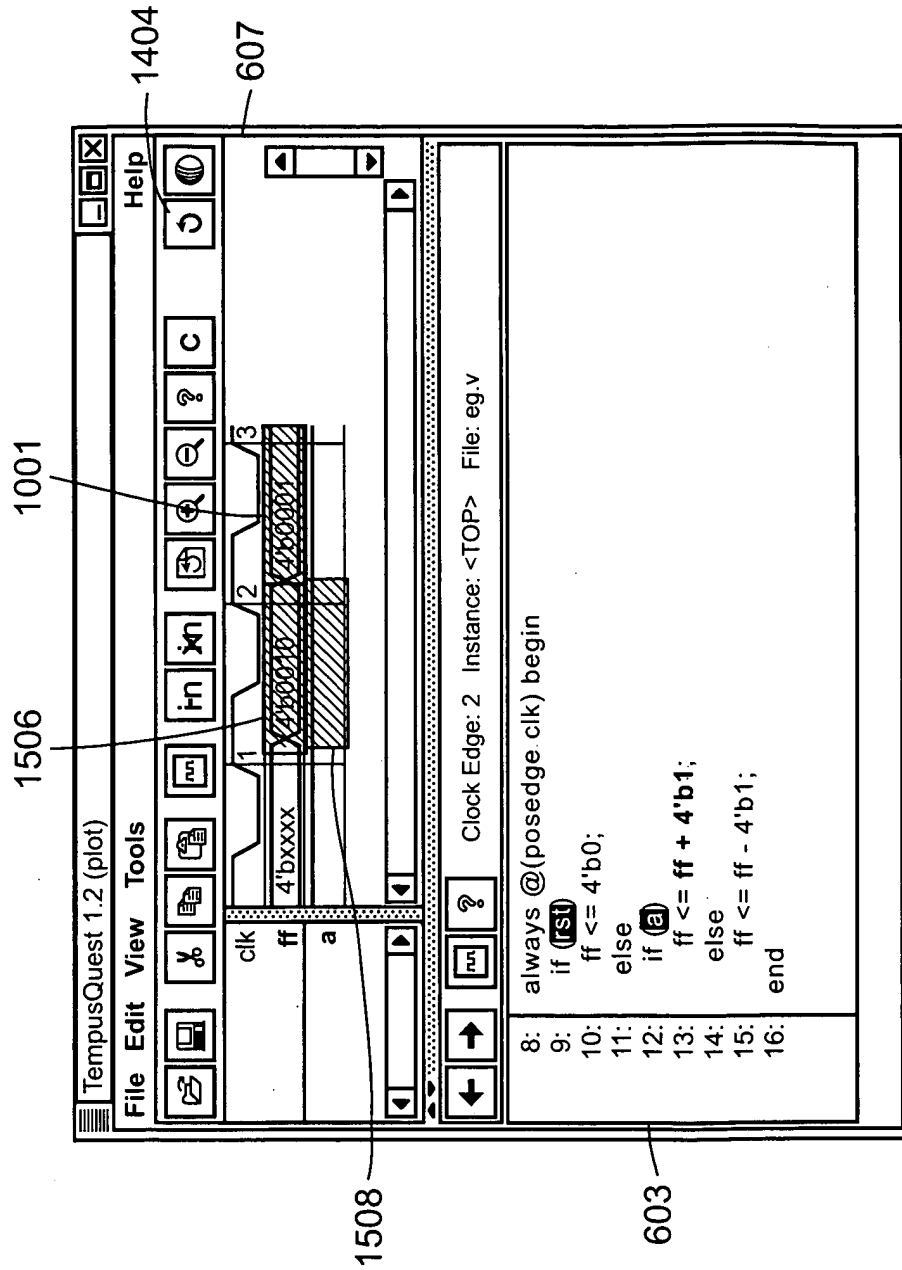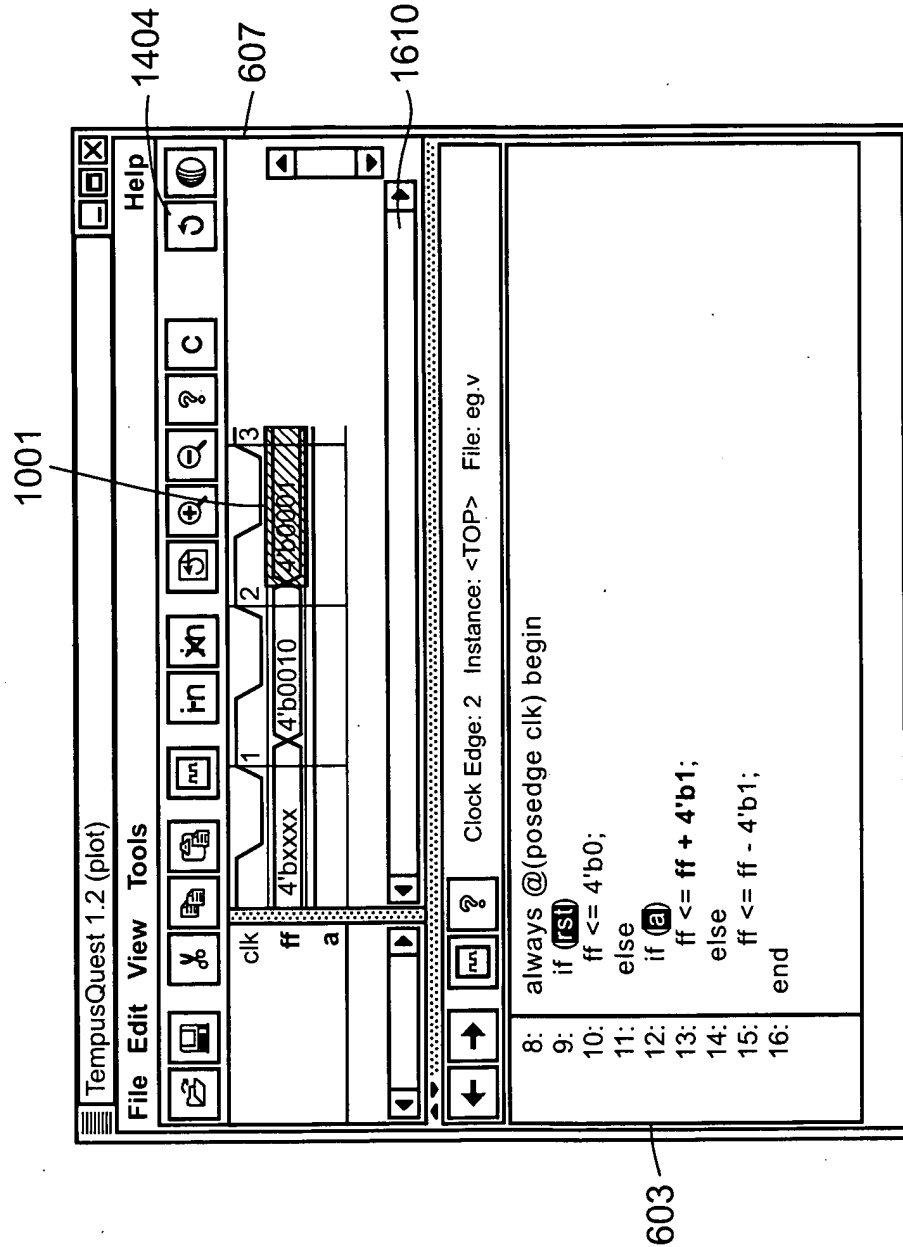Atty. Docket No.: 24006-08742

FIG. 16